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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHAN, ALEX H	

ART UNIT	PAPER NUMBER
2633	3

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/845,243	BOWLER ET AL.	
	Examiner	Art Unit	
	Alex H Chan	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "transmitter in a Passive Optical Network" in claim 7 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claim 5** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, claim 5 recites "the power level" of claim 3 where there is insufficient antecedent basis for this limitation in the claim. Also, it is not clear to which power level the applicant is referring.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claim 1** is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,232,842 B1 to Asano.

Regarding claim 1, Asano discloses a burst mode receiver (Col. 30, lines 38-41) comprising: a converter (91 of Fig. 11) which converts a received optical signal into an electrical signal; a pre-amplifier (92 of Fig. 11) coupled to the converter, which receives the electrical signal from the converter and outputs a corresponding voltage signal (Col. 27, lines 26-31 and Col. 33, lines 43-52), the voltage signal (e.g. 1201, 1202 or 1203 of Fig. 12a and 12b) having a driven edge time constant for each driven edge of the electrical signal and an undriven edge time constant that is extended and longer than the driven edge time constant for each undriven edge of the electrical signal (e.g. the time constant for a driven edge (e.g. the 1st pulse) of 1201 of Fig. 12a is less than the time constant for an undriven edge (decaying state of 4th pulse) of 1202 of Fig. 12b); and a differential amplifier (15 of Fig. 11) having a hysteresis circuit (97 of Fig. 11) coupled to the preamplifier, the differential amplifier receiving the voltage signal from the preamplifier (via 1202 and 1203 of Fig. 11, Col. 27, lines 49-53) and outputting a digital signal (1210 of Fig. 11, Col. 28, lines 21-25) corresponding to the voltage signal (Col. 28, lines 20-22),

wherein hysteresis circuit holds the digital signal in a particular state for each undriven edge of the voltage signal and changes the state of the digital signal for each driven edge of the voltage signal (e.g. when 1201 of Fig. 12a is "high," 1210 of Fig. 12e outputs a logic "1" whereas when 1201 of Fig. 12a is "low," 1210 of Fig. 12e outputs a logic "0").

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,892,6098,to Saruwatari in view of U.S. Patent No. 6,232,842 B1 to Asano.

Regarding claim 1, Saruwatari discloses a burst mode receiver (Col. 1, lines 4-5) comprising: a converter (1 of Fig. 8) which converts a received optical signal into an electrical signal; a pre-amplifier (2 of Fig. 8) coupled to the converter, which receives the electrical signal from the converter and outputs a corresponding voltage signal (V_+ and V_-/ V_{m+} and V_{m-}), the voltage signal having a driven edge time constant for each driven edge of the electrical signal and an undriven edge time constant that is extended and longer than the driven edge time constant for each undriven edge of the electrical signal (e.g. the time constant for a driven edge (e.g. the 1st pulse) of V_+ of Fig. 15b is less than the time constant for an undriven edge (decaying

state of 2nd pulse till the rise of the 3rd pulse) of V_+ of Fig. 15b or the time constant for a driven edge (e.g. the 1st pulse) of V_{m+} of Fig. 15c is less than the time constant for an undriven edge (decaying state of 3rd pulse) of V_{m+} of Fig. 15c); and a differential amplifier (13 and 14 of Fig. 8) having a hysteresis circuit (7 of Fig. 8) coupled to the preamplifier, the differential amplifier receiving the voltage signal (V_{p+} and V_{p-}) from the preamplifier. Saruwatari does not explicitly disclose a differential amplifier receiving the voltage signal and outputting a digital signal corresponding to the voltage signal, wherein hysteresis circuit holds the digital signal in a particular state for each undriven edge of the voltage signal and changes the state of the digital signal for each driven edge of the voltage signal. Asano discloses an differential amplifier receiving the voltage signal from the preamplifier (via 1202 and 1203 of Fig. 11, Col. 27, lines 49-53) and outputting a digital signal (1210 of Fig. 11, Col. 28, lines 21-25) corresponding to the voltage signal (Col. 28, lines 20-22), wherein hysteresis circuit holds the digital signal in a particular state for each undriven edge of the voltage signal and changes the state of the digital signal for each driven edge of the voltage signal (e.g. when 1201 of Fig. 12a is "high," 1210 of Fig. 12e outputs a logic "1" whereas when 1201 of Fig. 12a is "low," 1210 of Fig. 12e outputs a logic "0"). Accordingly, one of the ordinary skill in the art would have been motivated to employ the above means for providing a comparator or hysteresis circuit which corrects and reproduces a reference pulse signal (Col. 3, lines 6-15), whereby distortion of pulse width can be suppressed (Col. 1, lines 48-54). Therefore, it would have been obvious to one of artisan skill in the art at the time the invention was made to modify the digital signal receiver of Saruwatari by incorporating a hysteresis circuit which holds the digital signal in a particular state for each undriven edge of

the voltage signal and changes the state of the digital signal for each driven edge of the voltage signal because it corrects and reproduces a reference pulse signal as taught by Asano.

Regarding claim 6, Asano discloses a filter (1411 and 1412 of Fig. 14) coupled between the pre-amplifier (92 of Fig. 11) and the differential amplifier (15 of Fig. 14).

8. **Claims 2-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Saruwatari in view of Asano as applied to claim 1 above, and further in view of U.S. Patent No. 5,430,765 to Nagahori.

Regarding claim 2, Saruwatari in view of Asano fails to disclose that the optical signal includes a plurality of packets transmitted in burst mode and the undriven edge time constant is shorter than a guard time between packets. Nagahori discloses an optical signal including a plurality of packets (Col. 8, line 23) transmitted in burst mode (Fig. 4) and the undriven edge time constant is shorter than a guard time between packets (e.g. the undriven edge time constant (decaying state) of Fig. 4b is within (i.e. shorter) bit interval, Col. 2, lines 31-33 and Col. 8, lines 17-22). One of the ordinary skill in the art would have been motivated to employ an optical signal including a plurality packet transmitted in burst mode and that the undriven edge time constant is shorter than a guard time between packets for preventing decision errors arouse due to spontaneous discharge during period of the subsequent pulse sequence (Col. 2, lines 20-33). Therefore, it would have been obvious to one of artisan skill in the art at the time the invention

was made to modify the digital signal receiver of Saruwatari in view of Asano by incorporating the above means for preventing decision errors as taught by Nagahori.

Regarding claim 3, Nagahori discloses that the optical signal includes a plurality of packets transmitted in continuous mode (e.g. via successive pulse sequences that space at sufficient amount of time interval by operating the receiver continuously (Col. 8, line 27).

Regarding claim 4, Nagahori discloses that the packets have a wide dynamic range of power level (e.g. via high and low amplitude pulses).

9. **Claims 5 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Saruwatari in view of Asano and Nagahori as applied to claim 3 above, and further in view of U.S. Patent No. 5,430,766 to Ota et al (hereinafter Ota).

Regarding claim 5 (as far as understood), Saruwatari in view of Asano and Nagahori does not explicitly disclose the power level is in the range –32dBm to –7dBm. Ota discloses that the power level of a packet is in the range –32dBm to –7dBm (e.g. –15dBm, Col. 1, lines 63-66). One of the ordinary skilled in the art would have been motivated to adjust the power level of a packet to a range of –32dBm to –7dBm for providing an optical receiver which can handle a wide range of packet amplitudes, separated by only a few nanoseconds in time (Col. 1, lines 66-

68). Therefore, it would have been obvious to one of artisan skill in the art at the time the invention was made to modify the digital signal receiver of Saruwatari in view of Asano and Nagahori by setting the power level in the range as described above because this provides an optical receiver which can handle a wide range of packet amplitudes. Also, since power level depends on the application specification and requirement, it would have been a matter of design choice to claim a power range as claimed by the applicant. This support rational is based on a recognition that the claimed differences exist not as a result of an attempt by applicant to solve a problem but merely amounts to selection of expedient known to the artisan of ordinary skill as design choice.

Regarding claim 7, Saruwatari in view of Asano, Nagahori and Ota discloses that the optical signal is received from a transmitter (Col. 3, line 65-Col. 4, lines 4, Ota) in a Passive Optical Network (e.g. optical subscriber systems or optical LANs, Col. 1, lines 4-7, Saruwatari).

10. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Saruwatari in view of Asano as discussed in claim 1 above, and further in view of U.S. Patent No. 5,430,766 to Ota et al (hereinafter Ota) or U.S. Patent No. 5,025,456 to Ota et al (hereinafter Ota).

Regarding claim 8, Saruwatari in view of Asano discloses all limitations as discussed in claim 1 above, but fails to disclose AC-coupling the electrical signal to provide an AC-couple signal. Ota (U.S. No. 5,430,766) discloses AC-coupling the electrical signal to provide an AC-

couple signal (e.g. via ac-coupling, Col. 1, lines 20-26). Ota discloses (U.S. No. 5,025,456) discloses AC-coupling the electrical signal to provide an AC-couple signal (e.g. via conventional ac-coupled optical receivers intended for continuous data transmission, Col. 1, lines 10-14). Accordingly, one of the ordinary skill in the art would have been motivated to ac-couple the electrical signal to provide an ac-couple signal because they work well with continuous data transmission (Col. 1, lines 30-31, Ota (U.S. No. 5,430,766)). Therefore, it would have been obvious to one of artisan skill in the art at the time the invention was made to modify the digital signal receiver of Saruwatari in view of Asano by ac-coupling the electrical signal to provide an ac-coupled signal because ac-coupling works well with continuous data transmission as taught by Ota.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kikuchi is cited to demonstrate a PON system (Fig. 4) and a differential amplifier comprising a comparator (Fig. 7) for holding states (Fig. 8). Nobuhara is cited to show another PON system with transmitter-receiver (Fig. 10) comprising an optical burst receiver having a pre-amplifier and differential units (Fig. 13). Nakamura et al is cited to show an optical communication (Fig. 1) comprising transmitter, and receivers having pre-amplifier and differential amplifier (Fig. 3 and 4) with driven and undriven edge time constant (Fig. 5A, 5B and 14). Nagahori (U.S Patent No. 5,838,731) (Fig, 2 and 4), Asano (U.S. Patent No. 5,875,049) (Fig. 9) and Yamashita (Fig. 6) are cited to show driven and undriven edge time constant. Uno is

cited to show a similar structure of an optical receiver (Fig. 2) having driven and undriven time constant (Fig. 10, 13 and 15). Masucci et al is cited to show burst mode transmission relative to time (Fig. 6-10). Akimoto et al is cited to show another PON system (Fig. 14) comprising packets with different peak and threshold value (Fig. 21).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alex H Chan whose telephone number is (703) 305-0340. The examiner can normally be reached on Monday to Friday (8am to 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (703) 305-4729. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Alex Chan
Patent Examiner, AU 2633
December 22nd, 2003

JASON CHAN
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